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GB 2297884 A GB 2297854 A EP 0586256 A2
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(54) Time Base Alignment for Digital Mobile Phones

(57) A digital mobile telecommunications station as shown in Figure 2 has a high frequency timebase circuit which can be synchronised with a base station timebase. Provision is made for shutting down the timebase for a period for power saving and for re-synchronising the timebase following completion of the shutdown period. The re-synchronising means includes a low frequency clock, a first counter (30) for counting cycles of the low frequency clock and second counter means (31) for counting cycles of a high frequency clock forming part of the timebase circuit. A first storage means (22a) stores the count in the second counter means at a first specified point in a timebase cycle during shutdown and a second storage means (22b) for storing the count in the second counter means at a second specified point in a timebase cycle following completion of shutdown. The timebase is connected after the shutdown on the basis of the number of cycles of the low frequency clock and the numbers stored in the first and second storage means.

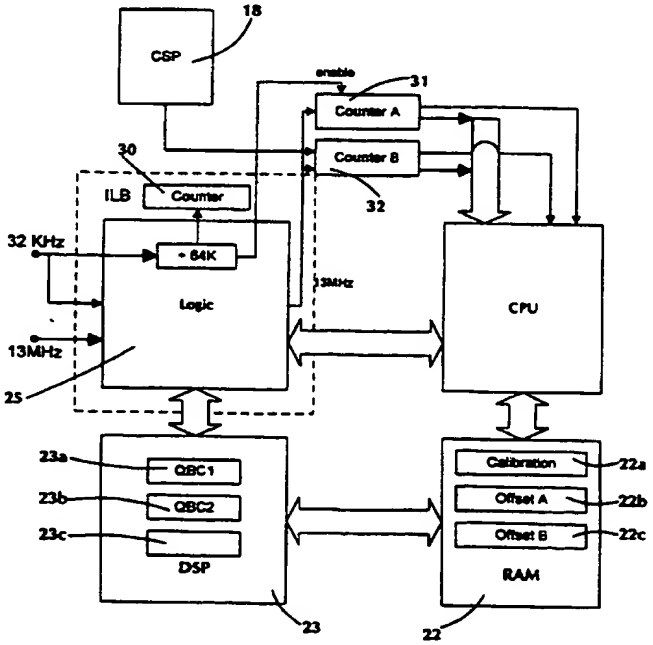

Figure 2

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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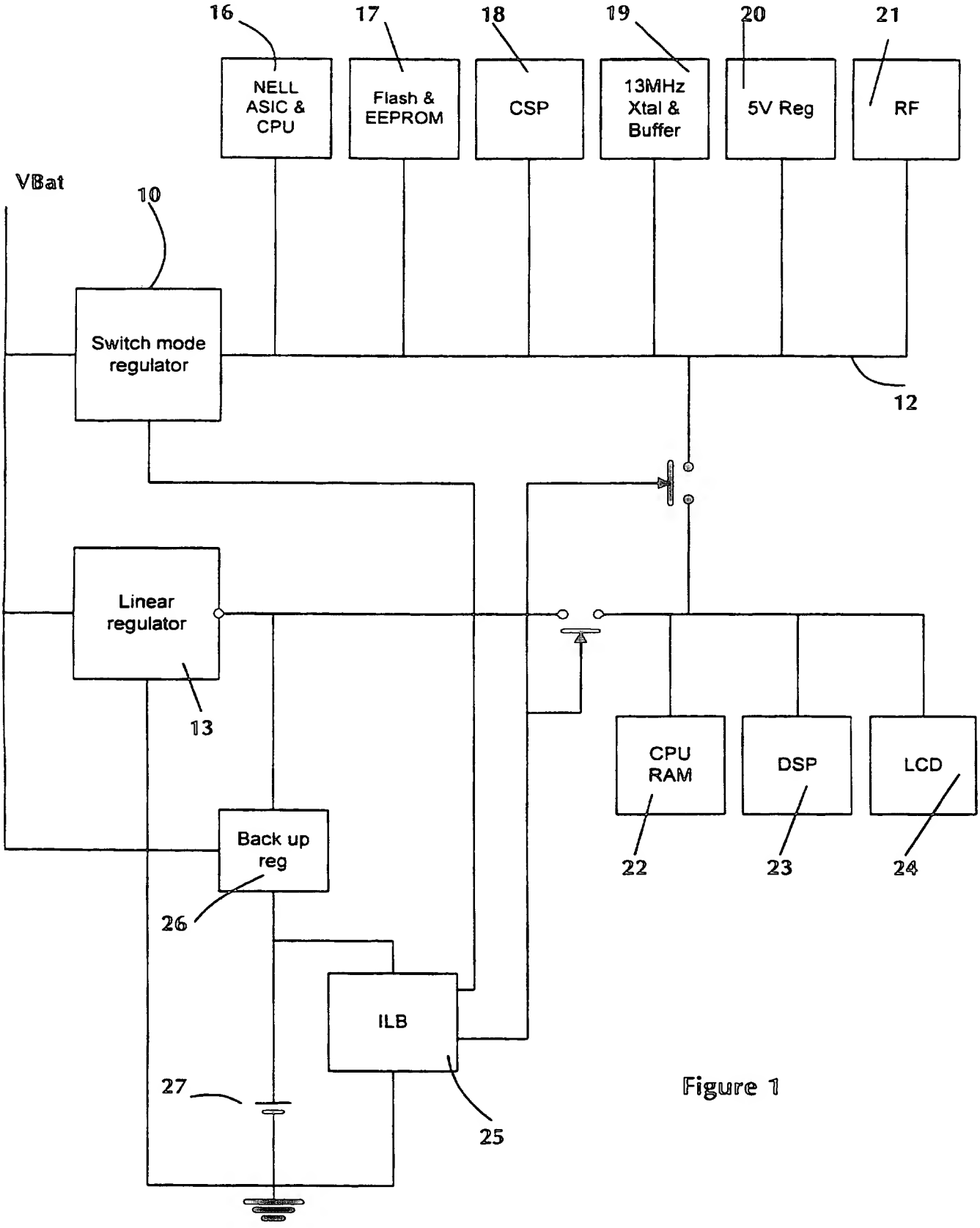

Figure 1

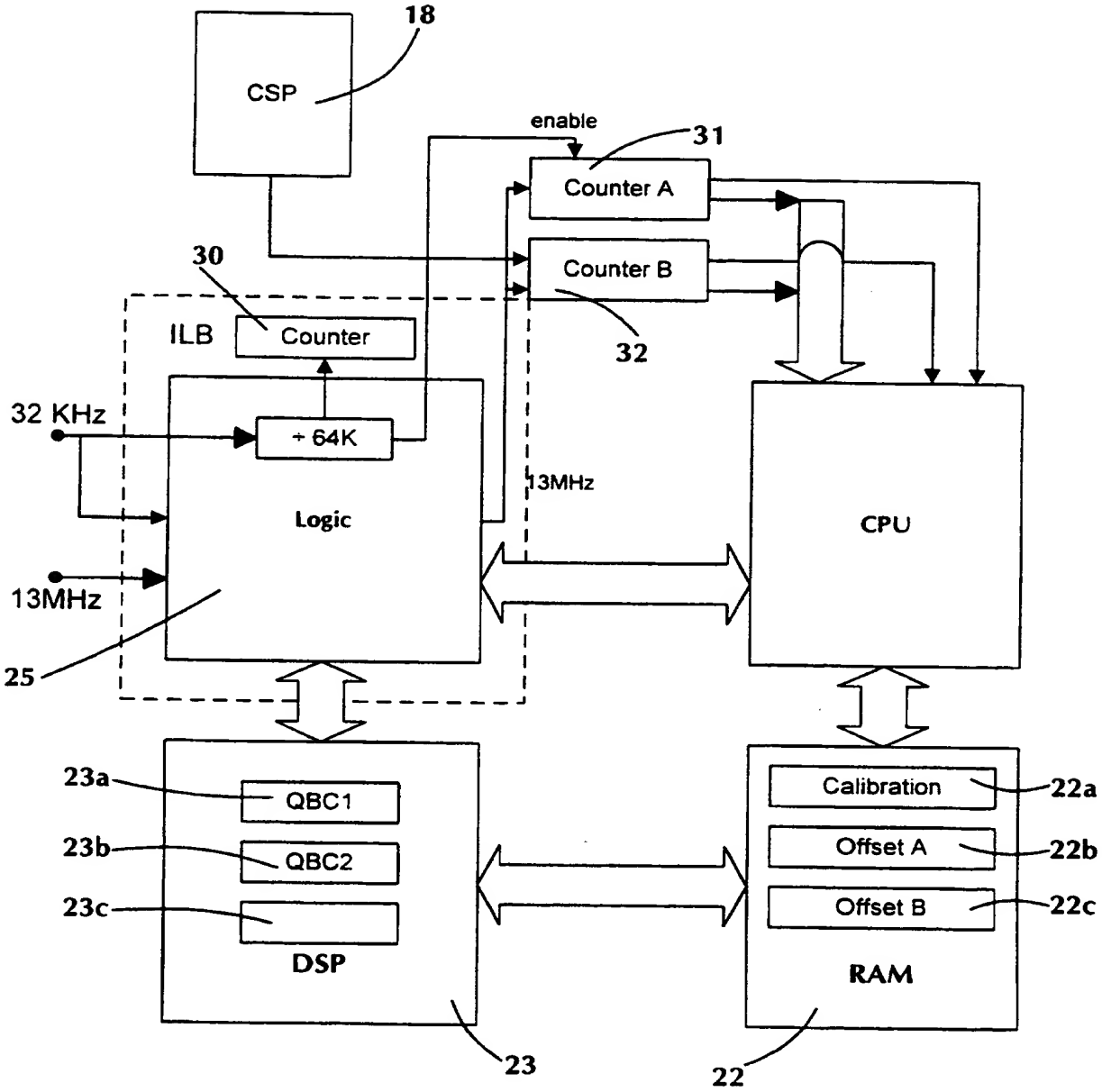

Figure 2

TIME BASE ALIGNMENT FOR DIGITAL MOBILE PHONES

Digital mobile phone systems (eg GSM phones) rely for their operation on accurate matching of a local timebase within a mobile station with the timebase of a base station. During idle or standby operation, the mobile phone must receive pages periodically, together with decoding broadcast information concerning the network configuration. For power-saving between these periods of activity it is desirable to shut down as much of the mobile station circuitry as possible and, as the timebase circuitry operates at a high frequency, for example 13 MHz in the GSM system, considerable power can be saved by shutting down the timebase circuitry during "sleep" periods.

However, re-synchronising the mobile station timebase with the base station timebase on re-awakening (e.g. for paging reception) needs to be accomplished quickly and it is therefore highly desirable to reconstruct the mobile station timebase in synchronism with its operation before shutdown without reference to the base station signals, or utilising the base station signals to reconstruct the time base takes time and uses considerable power.

It is therefore an object of the present invention to provide a digital mobile telecommunication station in which there is provision for timebase reconstruction after a power-saving shut down.

In accordance with the invention, there is provided a digital mobile telecommunications station having a high frequency timebase circuit which can be synchronised with a base station timebase, means for shutting down said high frequency timebase circuit for a predetermined period for power saving purposes, and means for re-synchronising the

timebase circuit following completion of the shut down period, said re-synchronising means including a relatively low frequency clock, a first counter for counting cycles of said low frequency clock, second counter means for counting cycles of a high frequency clock forming part of the timebase circuit, first storage means for storing the count in said second counter means at a first specified point in a timebase cycle during shutdown, second storage means for storing the count in said second counter means at a second specified point in a timebase cycle following completion of the shut down and means for correcting the timebase after such completion on the basis of the number of cycles of the low frequency clock for which shut down persisted, the numbers stored in said first and second storage means and data identifying said first and second points in the timebase cycles referred to.

In the accompanying drawings, Figure 1 is a block diagram showing the power supply arrangements of one example of a mobile telecommunication station in accordance with the present invention, and Figure 2 is a block diagram of the timebase re-synchronisation means included in the mobile station.

As shown in Figure 1, the mobile phone apparatus includes a main switch-mode power supply regulator 10 which controls the supply of power from a main battery 11 to a main 3.0V supply bus 10. There is also a lower power linear power supply regulator 13 which is used to supply power to some of the components of the mobile station during power-saving operation.

Power for all the power consuming circuits of the mobile station is provided in normal operation by the main regulator 10. These circuits

include an ASIC 16 (including a CPU), flash and EEPROM memory 17, and a CSP unit which provides many of the functions of the mobile station such as Tx modulation, DAC services, Rx filtering, DC calibration, ADC services, audio processing and GSM time base counters. The CSP unit 18 is connected to the audio circuits (not shown) of the phone. A 13 MHz crystal oscillator and buffer circuit 19 which provides a high frequency clock for the system, a 5V regulator 20 (for the SIM and audio circuits), and the RF circuits 21 of the phone apparatus are also supplied directly by the bus 12. Power for the CPU RAM unit 22, for the DSP unit 23 (which provides algorithm implementation, speech encoding and decoding and other services), and for an LCD display 21 is also normally supplied from the bus 12, but from the low power linear regulator 13 during power-saving operation.

Connection of the RAM 22, the DSP 23 and the LCD to the two power supply regulators is controlled by two switch devices under the control of an independent logic block (ILB) 25 which is continuously powered by a back-up regulator and/or a back-up battery 27. The ILB is, in fact, a part of the ASIC, but is electrically isolated from the remainder of the ASIC. The ILB also controls operation of the switch mode regulator 10 and can turn it off and on as required.

In addition to the 13 MHz clock oscillator which is used for synchronising operation of the mobile station with the signals transmitted from a base station, there is also a 32 KHz oscillator (actually employing a 32768 Hz crystal) which is used for the timing of the "sleep" periods, whilst the main 13 MHz clock oscillator is powered down. As shown in Figure 2, the ILB 25 includes a first counter 30 for counting pulses from

the 32 KHz sleep clock. To allow for drift in the frequency of the 32 KHz clock period re-calibration thereof is needed.

The calibration operation involves the use of a calibration counter 31 which is controlled by a ÷64 K block in the ILB to count 13 MHz clocks for a period of 2 seconds determined in accordance with the 32 KHz clock. Under the control of the ILB, the count of the counter 31 at the end of the 2 second calibration period is transferred by the CPU to a specific RAM storage location 22^a. The counter 31 is expected at the end of each calibration count to contain a count of exactly 26M, and any offset from this is taken as indicating an error in the frequency of the 32KHz clock. The count in counter 31 at the end of each two second calibration period is compared with that stored in the last calibration period. If the difference exceeds a predetermined threshold a flag is set by the CPU to indicate that the 32KHz clock is still not settled and inhibit power saving sleep operation. This ensures that drift of the 32KHz clock frequency following power-up or the making or receiving of a call does not prevent time base reconstruction.

As shown in Figure 2 the ASIC also contains a second counter means comprising a counter 33, which is used to count 13 MHz clocks under the control of the ILB during the operations required to commence sleep mode and at the end of the sleep mode at specific quarter (or eighth) bit numbers in the GSM timebase created from the 13 MHz clock. The offset counts from these two counters are stored in two specific RAM locations 22^b and 22^c as will be described hereinafter.

In operation, when the CPU has determined that a sleep period is possible, the CPU first issues a command to the DSP that the sleep

period is to be commenced and then awaits a handshake confirmation from the DSP to confirm that sleep mode has been commenced. At this stage, the CPU provides the ILB with data specifying the duration of the required wait between turning on of the 13 MHz clock at re-awakening and restarting of the CPU, data specifying the duration of the required wait between restarting of the CPU and the sending of a CPU interrupt, and data specifying the required wait between the sending of the interrupt and the recapture of the GSM timebase. The CPU supplies to the ILB a digital signal representing the required during of the sleep period measured in cycles of the 32 KHz clock. The ILB sends a vectored interrupt to the DSP on the next rising edge of the 32 KHz clock. Simultaneously, the rising edge of the 32 KHz clock causes the starting of the counters 30 and 32, which count 32 KHz and 13 MHz clocks respectively.

On receipt of the vectored interrupt from the ILB, the DSP issues a command to the CSP to assert an OCTL line at QBC+2 and an interrupt to the DSP at QBC+3. The DSP stores the QBC value which will trigger OCTL in its own RAM location 23[a]. Following reception of the CSP interrupt, the DSP enters clock stopped mode. Assertion of the OCTL line by the CSP stops the counter 32 and causes the CPU to read the value stored in counter 32 and write it to the RAM location 22[b]. The CPU then instructs the ILB to enter sleep mode and itself enters HALT mode. The ILB first removes power from the 13 MHz buffer and then turns off the switch-mode power supply, leaving the RAM 22, the DSP 23 and the LCD 24 powered by the linear power supply regulator 13 only.

Wake-up from sleep mode commences either at the expiry of the predetermined number of 32 KHz cycles or on detection of an asynchronous event such as the pressing of a key on the mobile station keypad. In either event the actual wake-up sequences commences at a rising edge of the 32 KHz clock, the next following an asynchronous event if this is what has triggered wake-up. At this time, the ILB switches on the switch-mode power supply regulator and, after a predetermined interval, enables the 13 MHz buffer. After a further predetermined period the ILB release the CPU reset and after yet a further interval it interrupts the CPU. The CPU then triggers waking up of the DSP via PHIF communications and instructs the DSP to reconstruct the GSM timebase. At the expiry of a timer the ILB interrupts the DSP. The rising edge of the 32 KHz clock which initiated the above-described actions also causes the ILB to reset and enable the 13 MHz counter 32 and stops the 32 KHz counter 30. The interrupt to the DSP triggers the loading in the CSP of an event QBC+2 to output an OCTL line. The assertion of the OCTL line stops the counter 32 and causes the CPU to read the sleep time in 32 KHz cycles from the ILB and to read the 13 MHz counter offset from power on into the RAM location 22^c, and the DSP saves the QBC+2 value into its own RAM location 23^b.

The CPU now passes to the DSP, the total sleep time in 32 KHz cycles, the two offset counts from the RAM locations 22^b and 22^c and the calibration count stored in the RAM location 22^a. The DSP now uses these values to perform all the necessary operations to reconstruct the GSM timebase in synchronism with the base station timebase. The DSP calculations involve

(i) determining the difference (δ) between the two offset count values from RAM locations 22^b and 22^c (divided by 12 to convert to QBM values),

(ii) adding this difference δ to the sleep duration calculated in QBM values,

(iii) adjusting the QBM value just calculated to allow for the current calibration of the 32KHz clock, by multiplying it by a value derived by dividing the value from RAM location 22^a by the product of the frequency (13×10^6) and the calibration period duration (2 in the present duration),

(iv) calculating an offset QBM value in accordance with a value stored in the DSP representing the ratio of the stored off air time base frequency to the on board 13MHz frequency, and

(v) adding this offset QBM value to the QBM value stored at RAM location 23^a.

CLAIMS

1. A digital mobile telecommunications station having a high frequency timebase circuit which can be synchronised with a base station timebase, means for shutting down said high frequency timebase circuit for a predetermined period for power saving purposes, and means for re-synchronising the timebase circuit following completion of the shut down period, said re-synchronising means including a relatively low frequency clock, a first counter for counting cycles of said low frequency clock, second counter means for counting cycles of a high frequency clock forming part of the timebase circuit, first storage means for storing the count in said second counter means at a first specified point in a timebase cycle during shutdown, second storage means for storing the count in said second counter means at a second specified point in a timebase cycle following completion of the shut down and means for correcting the timebase after such completion on the basis of the number of cycles of the low frequency clock for which shut down persisted, the numbers stored in said first and second storage means and data identifying said first and second points in the timebase cycles referred to.

2. A digital mobile telecommunications station as claimed in claim 1, in which said first and second specific points in the timebase cycles are specific quarter (or eighth) bit numbers in the timebase cycles.

3. A digital mobile telecommunications station as claimed in Claim 1 or Claim 2, further comprising calibration means for periodic calibration of the said low frequency clock against said high frequency clock, said timebase correction means taking such calibration into account when correcting the time base.

4. A digital mobile telecommunications station as claimed in Claim 3, in which said calibration means comprises a counter for counting pulses from said high frequency clock for a period determined by said low frequency clock and means for storing the count from said counter for use by said timebase correction means.

The Patent Office

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Claims searched: all **Date of search:** 4 March 1997

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4L (LECTP); G4H (HRCA)

Int Cl (Ed.6): H04Q 7/18, 7/32; H04M 1/72

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2297884 A	(NOKIA) See whole document	1-4
A	GB 2297854 A	(NOKIA)	
X	EP 0586256 A2	(NOKIA) See whole document	1-4
A	EP 0343528 A2	(FUJITSU)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.